FAIRCHILD SEMICONDUCTOR®

May 2007

CD4040BC, 12-Stage Ripple Carry Binary Counters
CD4060BC, 14-Stage Ripple Carry Binary Counters

Features

- Wide supply voltage range: 3.0V to 15V
- High noise immunity: 0.45 V_{DD} (Typ.)
- Low power TTL compatibility: Fan out of 2 driving 74L or 1 driving 74LS
- Medium speed operation: 8MHz typ. at V_{DD} = 10V
- Schmitt trigger clock input

General Description

The CD4060BC is a 14-stage ripple carry binary counter, and the CD4040BC is a 12-stage ripple carry binary counter. The counters are advanced one count on the negative transition of each clock pulse. The counters are reset to the zero state by a logical “1” at the reset input independent of clock.

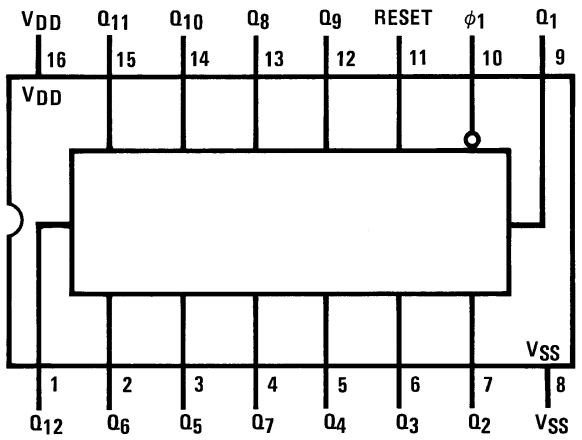
Ordering Information

Order Number	Package Number	Package Description
CD4040BCM	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
CD4060BCM	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
CD4060BCN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter “X” to the ordering number.

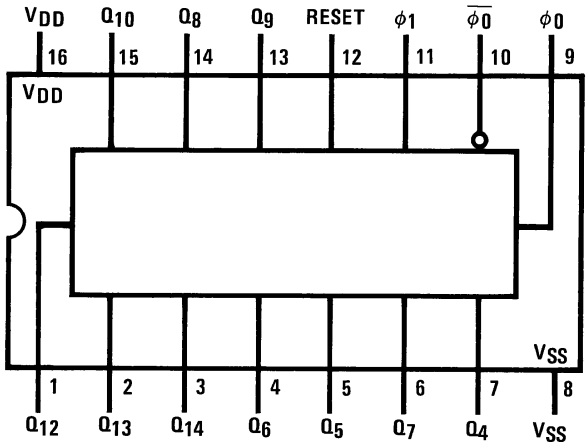
Connection Diagrams

Pin Assignments for DIP and SOIC
CD4040BC



Top View

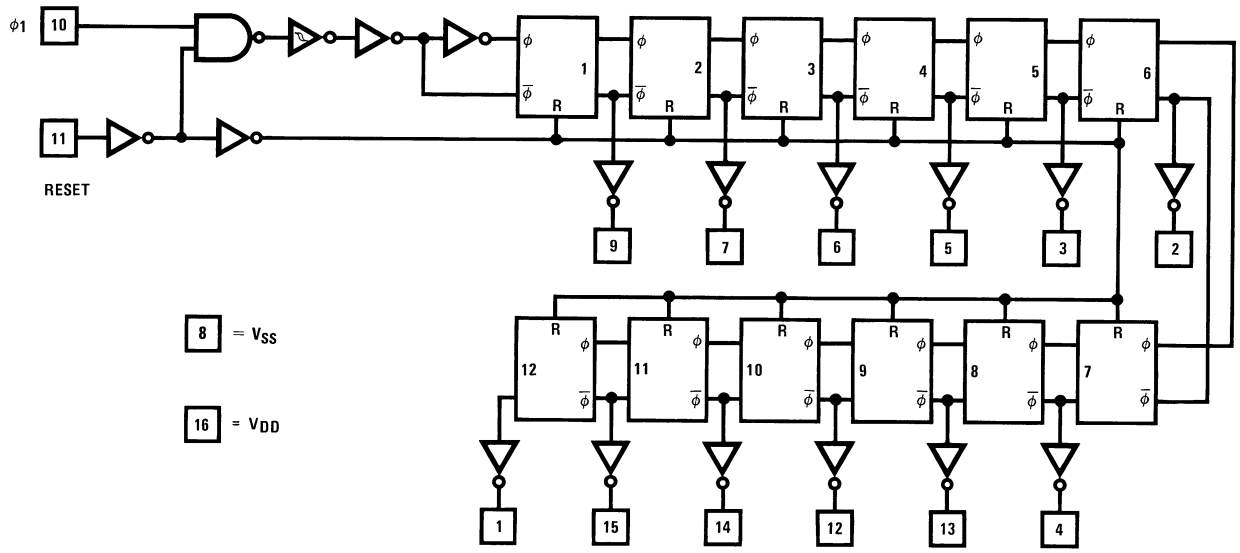
Pin Assignments for DIP and SOIC
CD4060BC



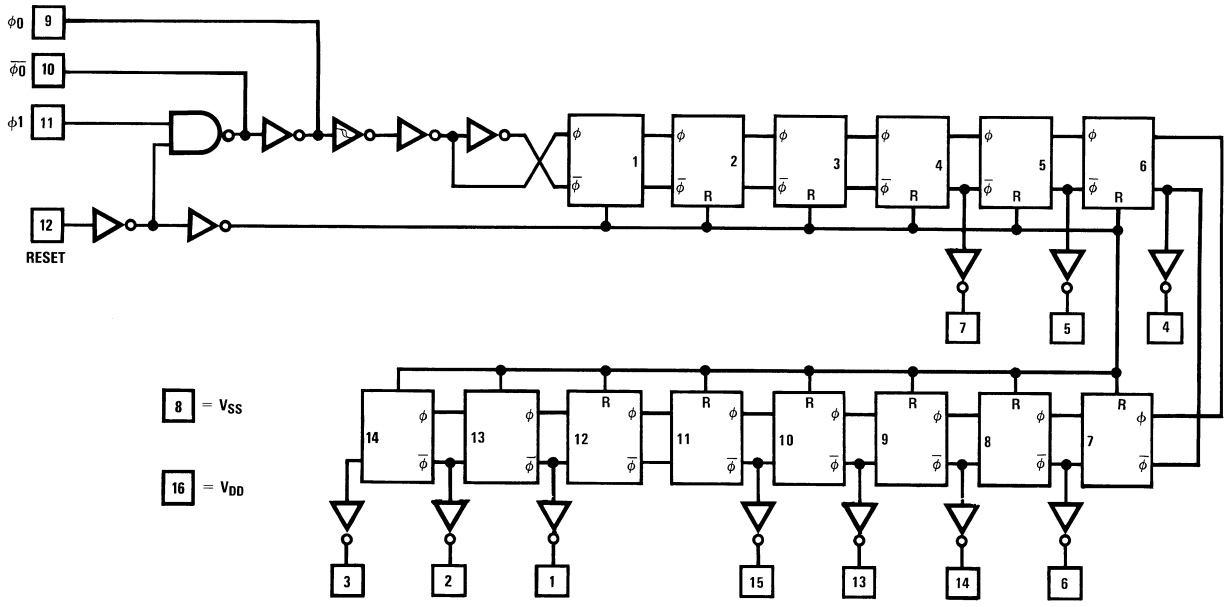
Top View

Schematic Diagrams

CD4040BC

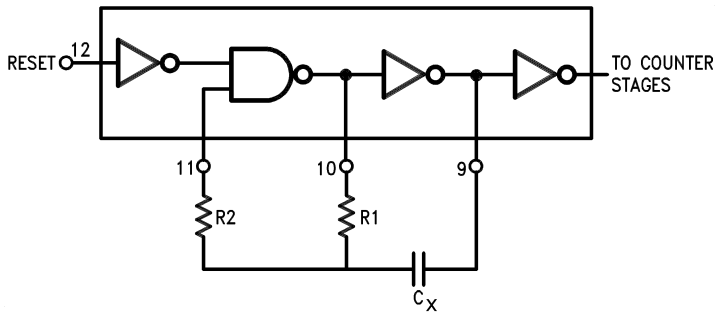


CD4060BC

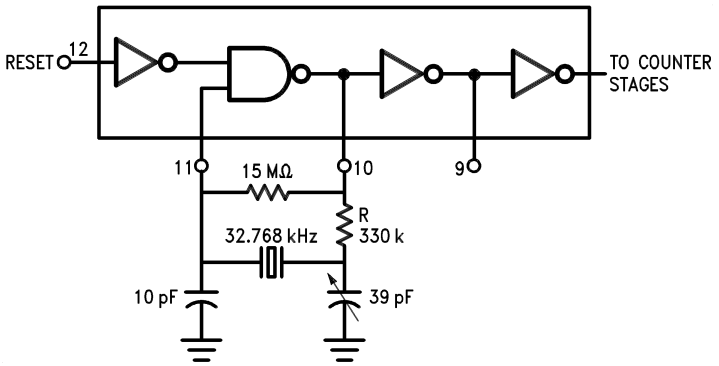


CD4060B Typical Oscillator Connections

RC Oscillator



Crystal Oscillator



Absolute Maximum Ratings[1]

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V_{DD}	Supply Voltage	–0.5V to +18V
V_{IN}	Input Voltage	–0.5V to V_{DD} +0.5V
T_S	Storage Temperature Range	–65°C to +150°C
P_D	Package Dissipation	
	N Package	700mW
	M Package	500 mW
T_L	Lead Temperature (Soldering, 10 seconds)	260°C

Note:

1. V_{SS} = 0V unless otherwise specified.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
V_{DD}	Supply Voltage	+3V to +15V
V_{IN}	Input Voltage	0V to V_{DD}
T_A	Operating Temperature Range	–55°C to +125°C

DC Electrical Characteristics[2]

Symbol	Parameter	Conditions	–55°C		+25°C			+125°C		Units
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		5			5		150	µA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		10			10		300	
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		20			20		600	
V_{OL}	LOW Level Output Voltage	V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	
		V_{DD} = 15V		0.05		0	0.05		0.05	
V_{OH}	HIGH Level Output Voltage	V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		
		V_{DD} = 15V	14.95		14.95	15		14.95		
V_{IL}	LOW Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2	1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0		4	3.0		3.0	
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6	4.0		4.0	
V_{IH}	HIGH Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	3		3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0	6		7.0		
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	9		11.0		
I_{OL}	LOW Level Output Current[3]	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		
I_{OH}	HIGH Level Output Current[3]	V_{DD} = 5V, V_O = 4.6V	–0.64		–0.51	–0.88		–0.36		mA
		V_{DD} = 10V, V_O = 9.5V	–1.6		–1.3	–2.25		–0.9		
		V_{DD} = 15V, V_O = 13.5V	–4.2		–3.4	–8.8		–2.4		
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		–0.1		-10^{-5}	–0.1		–1.0	µA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	

Note:

2. V_{SS} = 0V unless otherwise specified.

3. Data does not apply to oscillator points ϕ_0 and $\overline{\phi_0}$ of CD4060BC. I_{OH} and I_{OL} are tested one output at a time.

AC Electrical Characteristics[4]

CD4040BC $T_A = 25°C$, $C_L = 50pF$, $R_L = 200k\Omega$, $t_r = t_f = 20$ ns, unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
t_{PHL1}, t_{PLH1}	Propagation Delay Time to Q_1	$V_{DD} = 5V$		250	550	ns
		$V_{DD} = 10V$		100	210	
		$V_{DD} = 15V$		75	150	
t_{PHL}, t_{PLH}	Interstage Propagation Delay Time from Q_n to Q_{n+1}	$V_{DD} = 5V$		150	330	ns
		$V_{DD} = 10V$		60	125	
		$V_{DD} = 15V$		45	90	
t_{THL}, t_{TLH}	Transition Time	$V_{DD} = 5V$		100	200	ns
		$V_{DD} = 10V$		50	100	
		$V_{DD} = 15V$		40	80	
t_{WL}, t_{WH}	Minimum Clock Pulse Width	$V_{DD} = 5V$		125	335	ns
		$V_{DD} = 10V$		50	125	
		$V_{DD} = 15V$		40	100	
t_{rCL}, t_{fCL}	Maximum Clock Rise and Fall Time	$V_{DD} = 5V$			No Limit	ns
		$V_{DD} = 10V$			No Limit	
		$V_{DD} = 15V$			No Limit	
f_{CL}	Maximum Clock Frequency	$V_{DD} = 5V$	1.5	4		MHz
		$V_{DD} = 10V$	4	10		
		$V_{DD} = 15V$	5	12		
$t_{PHL(R)}$	Reset Propagation Delay	$V_{DD} = 5V$		200	450	ns
		$V_{DD} = 10V$		100	210	
		$V_{DD} = 15V$		80	170	
$t_{WH(R)}$	Minimum Reset Pulse Width	$V_{DD} = 5V$		200	450	ns
		$V_{DD} = 10V$		100	210	
		$V_{DD} = 15V$		80	170	
C_{IN}	Average Input Capacitance	Any Input		5	7.5	pF
C_{PD}	Power Dissipation Capacitance			50		pF

Note:

4. AC Parameters are guaranteed by DC correlated testing.

AC Electrical Characteristics[5]

CD4060BC $T_A = 25°C$, $C_L = 50pF$, $R_L = 200k$, $t_r = t_f = 20$ ns, unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
t_{PHL4}, t_{PLH4}	Propagation Delay Time to Q_4	$V_{DD} = 5V$		550	1300	ns
		$V_{DD} = 10V$		250	525	
		$V_{DD} = 15V$		200	400	
t_{PHL}, t_{PLH}	Interstage Propagation Delay Time from Q_n to Q_{n+1}	$V_{DD} = 5V$		150	330	ns
		$V_{DD} = 10V$		60	125	
		$V_{DD} = 15V$		45	90	
t_{THL}, t_{TLH}	Transition Time	$V_{DD} = 5V$		100	200	ns
		$V_{DD} = 10V$		50	100	
		$V_{DD} = 15V$		40	80	
t_{WL}, t_{WH}	Minimum Clock Pulse Width	$V_{DD} = 5V$		170	500	ns
		$V_{DD} = 10V$		65	170	
		$V_{DD} = 15V$		50	125	
t_{rCL}, t_{fCL}	Maximum Clock Rise and Fall Time	$V_{DD} = 5V$			No Limit	ns
		$V_{DD} = 10V$			No Limit	
		$V_{DD} = 15V$			No Limit	
f_{CL}	Maximum Clock Frequency	$V_{DD} = 5V$	1	3		MHz
		$V_{DD} = 10V$	3	8		
		$V_{DD} = 15V$	4	10		
$t_{PHL(R)}$	Reset Propagation Delay	$V_{DD} = 5V$		200	450	ns
		$V_{DD} = 10V$		100	210	
		$V_{DD} = 15V$		80	170	
$t_{WH(R)}$	Minimum Reset Pulse Width	$V_{DD} = 5V$		200	450	ns
		$V_{DD} = 10V$		100	210	
		$V_{DD} = 15V$		80	170	
C_{IN}	Average Input Capacitance	Any Input		5	7.5	pF
C_{PD}	Power Dissipation Capacitance			50		pF

Note:

5. AC Parameters are guaranteed by DC correlated testing.

RC Oscillator Notes:

1. $R_2 = 2\ R_1$ to $10\ R_1$
2. RC Oscillator applications are not recommended at supply voltages below 7.0V for $R_1 < 50k\Omega$
3. $f \approx \dfrac{1}{2.2\ R_1\ C_X}$ at $V_{CC} = 10V$

Physical Dimensions

Dimensions are in millimeters unless otherwise noted.

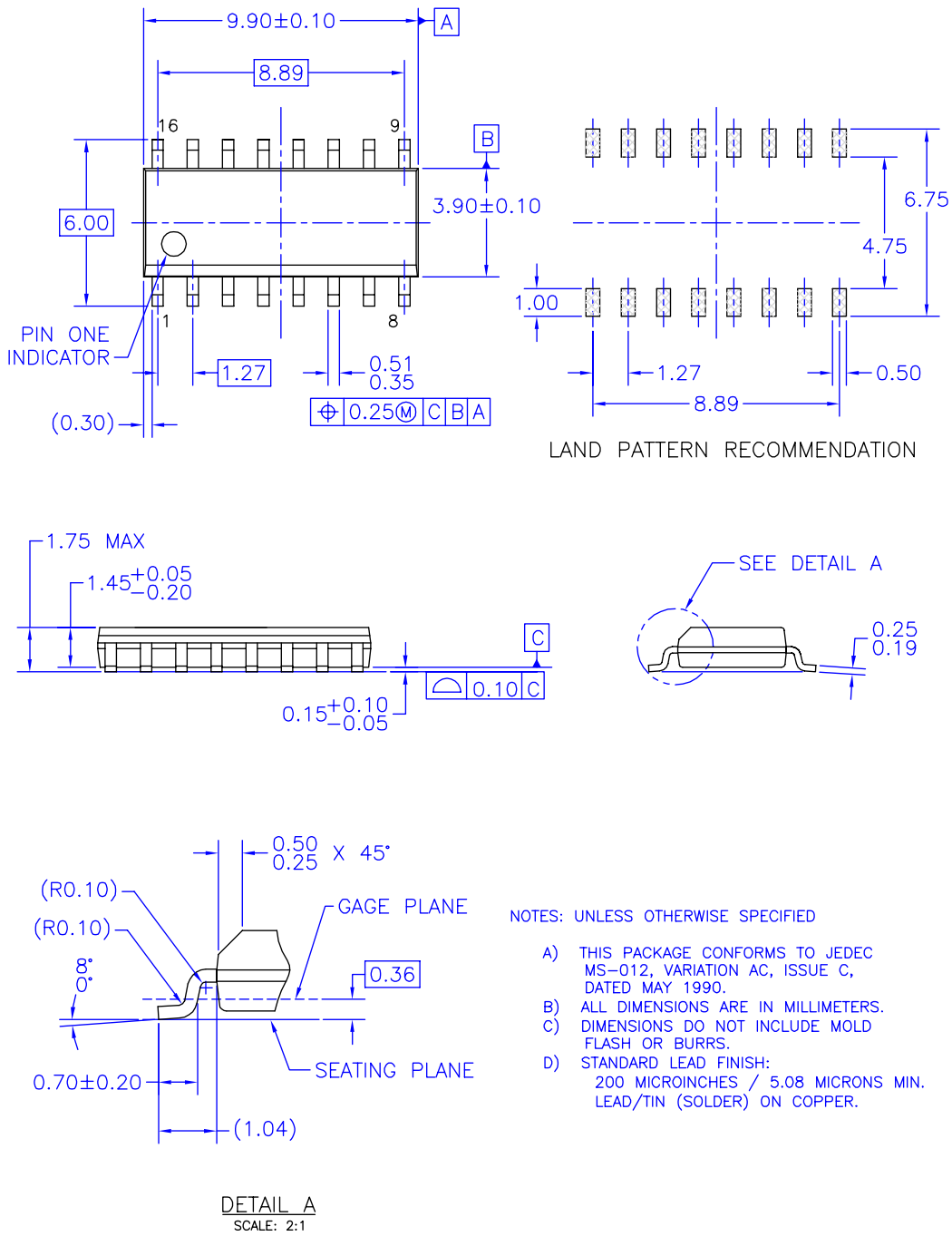


Figure 1. 16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Package Number M16A

Physical Dimensions (Continued)

Dimensions are in inches (millimeters) unless otherwise noted.

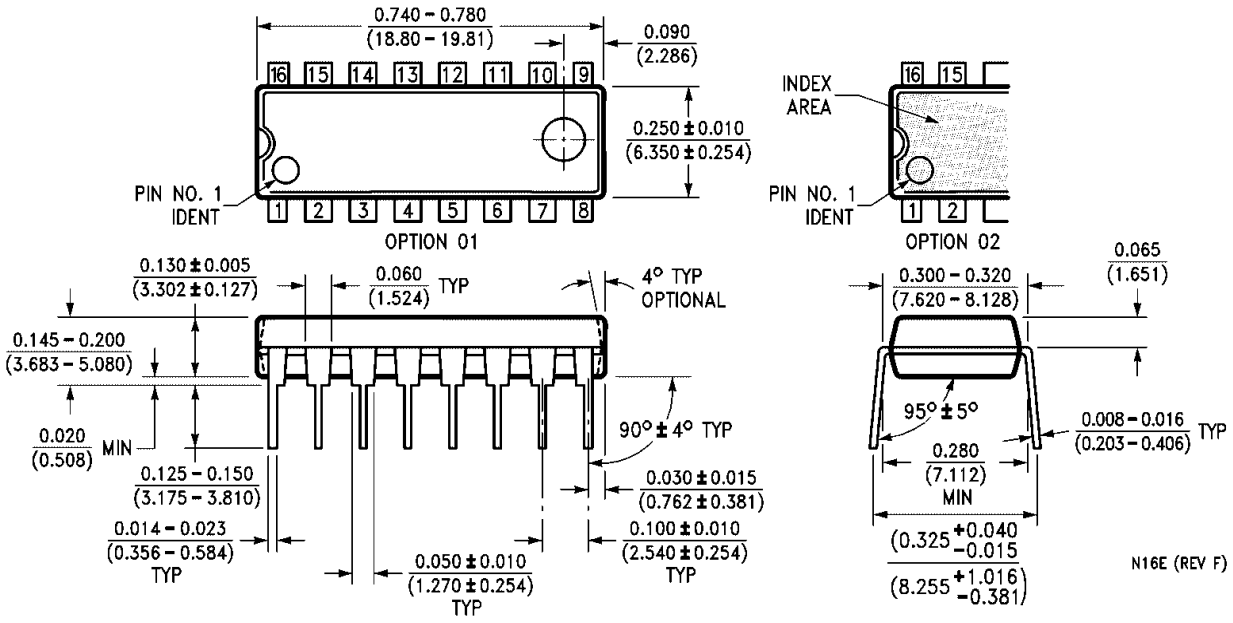


Figure 2. 16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N16E

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